REMARKS/ARGUMENTS

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on March 3, 2006. This Response has been prepared to reflect comments and suggestions made by the Examiner during the interview.

Amendments were made to the specification to complete the identification of related art referred to therein and to correct a noted error. No new matter has been added by any of the amendments to the specification.

A new title that is clearly indicative of the invention to which the claims are directed has been provided as required by the Examiner.

Claims 1-53 are pending in the present application. Claims 1, 12, 20, 22, 31, 33, 41 and 44 were amended. No claims have been added and no claims have been canceled. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims currently in the case patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 7, 12-13, 18, 22-23, 28, 33, 39, 44-46, and 51 under 35 U.S.C. § 102(b) as being anticipated by Hammond et al. (U.S. Patent No. 6,408,386 B1). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> In regard to claims 1, 12, 22, 33, 34, Hammond et al. discloses a method of processing performance information in a data processing system (see abstract), comprising the steps of: receiving an interrupt signal at an interrupt unit of a processor of the data processing system (see figure 5a &b, col. 9, lines 57 through col. 10, line 48); determining if at least one of a pre handler routine and a post handler routine are enabled for an interrupt (see col. 10, lines 29-49); invoking the pre handler routine to record events at a first instant if the pre routine is enabled (see col. 10, lines 36-42); invoking an interrupt handler routine (see col. 10, lines 36-42); and invoking the post handler routine to record events at a second instant if the post handler routine is enabled (see col. 10, lines 42-48.

Office Action dated December 8, 2005, pages 2-3.

Claim 1 of the present application, as amended herein, is as follows:

1. A method of processing performance information in a data processing system, comprising the steps of:
receiving an interrupt signal at an interrupt unit of a processor of the data processing system;
determining if at least one of a pre handler routine and a post handler routine are enabled for an interrupt;
invoking the pre handler routine to record events at a first instant if the pre handler routine is enabled;
invoking an interrupt handler routine following execution of the pre handler routine; and
invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). Applicants respectfully submit that Hammond et al. does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Hammond et al, (hereinafter "Hammond") does not disclose or suggest "invoking the pre handler routine to record events at a first instant if the pre handler routine is enabled", "invoking an interrupt handler routine following execution of the pre handler routine"; and invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled"; and, accordingly, does not anticipate claim 1.

Col. 10, lines 3-47 of Hammond, referred to by the Examiner in rejecting the claims reads as follows:

FIG. **5b** is a block diagram illustrating the information used by the event handling units while operating in the configuration shown in FIG. **5a** according to one embodiment of the invention. FIG. **5b** shows interrupt descriptor table **410**, handler **400a**, and an event handler region **510**. Event handler region **510** includes section **520** storing handler **500a** and section **530** storing handler **500b**. Interrupt descriptor table **410** includes entry **420** storing gate **512** and entry **430** storing intercept gate **435**. Thus, comparing FIGS. **4b** and **5b**, the contents of entry **430** in FIG. **4b** have been replaced with intercept gate **435** in FIG. **5b**.

> As previously described with reference to one embodiment of the invention, event handling unit **243** uses an event handler region which is divided into sections. One or more events are assigned to each section of the event handler region, and each section stores a handler for servicing its corresponding events. Upon the delivery of an event, event handling unit **243** stores event information identifying which event has occurred, calculates the address of the section of the event handler region to which the event corresponds, and causes the execution of the handler stored in that section. To calculate the address of the appropriate section, event handling unit **243** adds to the base address (i.e., the starting address) of the event handler region the event's corresponding section number multiplied by a predetermined value (e.g., **256**).
>
> When an exception generated by instruction set configuration **210** is received by event handling unit **233**, event handling unit **233** accesses a gate from interrupt descriptor table **410** as previously described. However, while in the configuration shown in FIG. **5a**, event handling unit **233** then inspects the accessed gate to determine whether it is a normal gate or an intercept gate. In one embodiment, this distinction is based on the state of an encoded bit field in the gate. A normal gate (e.g., gate **425**) contains the address of the exception's corresponding service routine (e.g., handler **400a**) according to the first system architecture. Upon accessing a normal gate, event handling unit **233** causes the processor to execute the handler identified by that gate (e.g., handler **400a**). In contrast, an intercept gate (e.g., intercept gate **435**) contains information identifying which event has occurred and that the event should be transferred to event handling unit **243**. Upon accessing an intercept gate, event handling unit **233** transfers event information (e.g., exception codes, vector numbers, etc.) to event handling unit **243**.

Hammond discloses a mechanism for providing event handling functionality in a computer system. The mechanism includes an event handling unit that has a plurality of event handlers. As described in col. 10, lines 16-19 of Hammond reproduced above, "One or more events are assigned to each section of the event handler region, and each section stores a handler for servicing its corresponding events." The present invention, on the other hand, is directed to providing pre and post handlers to record the occurrence of performance monitoring events before and following execution of an interrupt handler routine by an interrupt handler. As pointed out, for example, on page 6, line 22 to page 7, line 7 of the present application:

> In an alternative embodiment, before the processor fetches instructions from the interrupt handler when an interrupt occurs, the mechanism of the present invention allows the pre handler to log trace records prior to entering the interrupt handler. The events recorded provide the state of the system when entering an interrupt handler.
>
> When the interrupt handler completes the interrupt service routine, the mechanism of the present inventions allows the post handler to record events and low level information, such as the number of instructions executed for an interrupt, before returning to normal execution. This low-level information may provide the state of the system when exiting an interrupt.

Hammond does not disclose or suggest a system that includes a pre handler routine and a post handler routine wherein an interrupt handler routine is invoked following execution of the pre handler routine, and the post handler routine is invoked following execution of the interrupt handler routine as required by claim 1. During the above-referenced telephone interview, the Examiner referred to Fig. 5a of Hammond, and suggested that event handling unit 233 could be construed as a pre interrupt handler, handlers 400a-i as an interrupt handler and event handling unit 243 as a post interrupt handler. Figure 5a is reproduced below for the convenience of the Examiner:

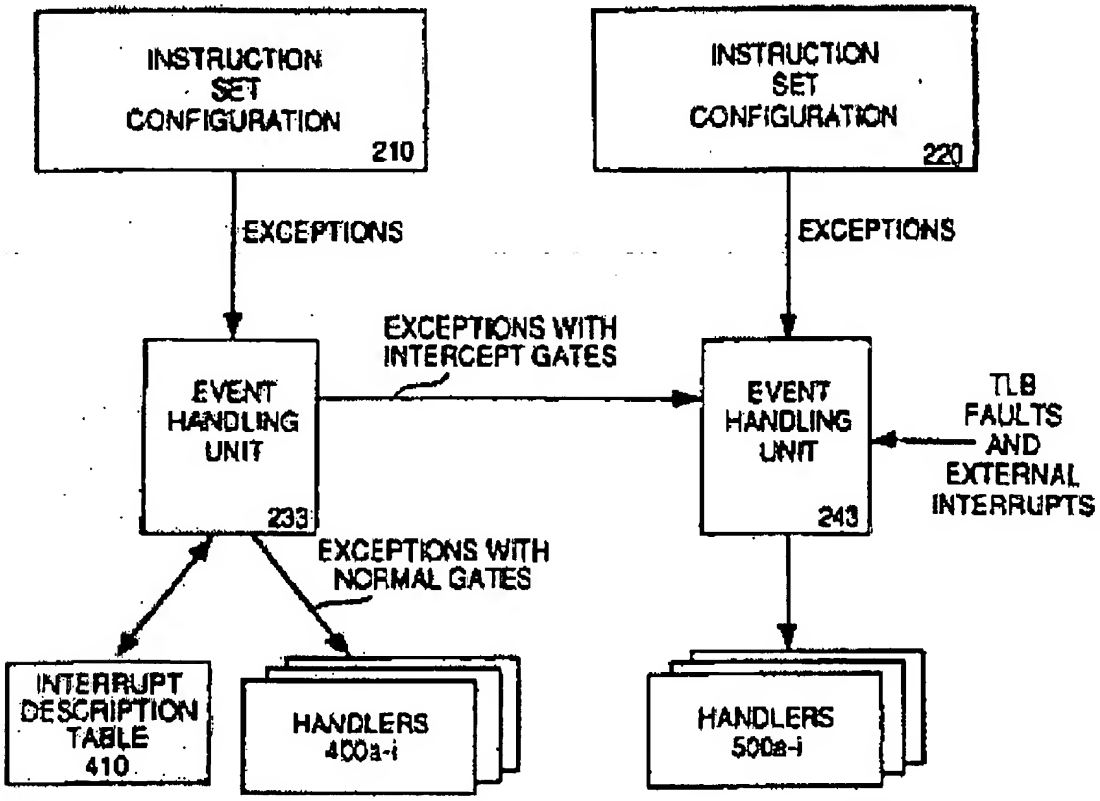

Figure 5a

As described in col. 10, lines 29-47 of Hammond reproduced above, event handling unit 233 functions to determine whether exceptions should be forwarded to handlers 400a-i or to event handling unit 243. This is also made clear from the arrows in Figure 5a which point from event handling unit 233 to handlers 400a-i and from event handling unit 233 to event handling unit 243. Assuming *arguendo* that event handling unit 233 can be construed as a pre handler, event handling unit cannot be construed as a

post handler wherein a post handler routine is invoked following execution of an interrupt handler routine. There is no arrow in Fig. 5a of Hammond that points from handlers 400a-i to event handling unit 243 which would be necessary, at the minimum, to attempt to construe unit 243 as a post handling unit.

In order to more clearly distinguish the present invention from the mechanism disclosed in Hammond, claim 1 has been amended to positively recite "invoking the pre handler routine to record events at a first instant if the pre handler routine is enabled", "invoking an interrupt handler routine following execution of the pre handler routine", and "invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled." These amendments make it clear that the interrupt handler routine is invoked following execution of the pre handler routine and that the post handler routine is invoked following execution of the interrupt handler routine. The event handling units in Hammond do not function in such sequential manner, and claim 1 is not anticipated by Hammond and patentably distinguishes over Hammond in its present form.

Claim 7 depends from and further restricts claim 1, and is also allowable in its present form, at least by virtue of its dependency.

Independent claims 12, 22, 33 and 44 have been amended in a manner similar to claim 1, and are also not anticipated by Hammond for substantially the same reasons as discussed above with respect to claim 1. Claims 13, 18, 23, 28, 39, 45, 46 and 51 depend from and further restrict one of independent claims 12, 22, 33 and 44 and are also not anticipated by Hammond, at least by virtue of their dependency.

Therefore, the rejection of claims 1, 7, 12-13, 18, 22-23, 28, 33, 39, 44-46, and 51 under 35 U.S.C. § 102 has been overcome.

Furthermore, Hammond does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Hammond teaches a plurality of event handlers for handling different events, and does not disclose a mechanism that includes a pre handler, an interrupt handler for handling events following execution of a pre handler routine, and a post handler for recording events following execution of an interrupt handling routine. Absent the Examiner pointing out some teaching or incentive to implement Hammond to achieve the present invention, one of ordinary skill in the art would not be led to modify Hammond to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Hammond in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' own disclosure as a template to make the necessary changes to reach the claimed invention.

II. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 2-6, 8-11, 14-17, 19, 24-27, 29-30, 35-38, 40, 42, 47-50, and 52-53 under 35 U.S.C. § 103(a) as being unpatentable over Hammond et al. (U.S. Patent No. 6,408,386 B1) in view of Levine et al. (U.S. Patent No. 5,691,920). This rejection is respectfully traversed.

In rejecting the claims, the Examiner acknowledges that Hammond does not disclose wherein recording events includes recording a plurality of counts, but asserts that Levine et al. (hereinafter "Levine") teaches a method and system for performance monitoring that includes recording a plurality of counts. Levine, however, does not supply the deficiencies in Hammond as discussed above, and the claims are allowable in their present form, at least by virtue of their dependency from allowable claims.

Therefore, the rejection of claims 2-6, 8-11, 14-17, 19, 24-27, 29-30, 35-38, 40, 42, 47-50, and 52-53 under 35 U.S.C. § 103 has been overcome.

III. Objection to Claims

The Examiner has stated that claims 20-21, 31-32, 41 and 43 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claims 20, 31 and 41 have been rewritten in independent form to incorporate all of the limitations of their base claim and intervening claims, and should now be allowed. Claims 21, 32 and 43 depend from and further restrict claims 20, 31 and 41, respectively, and should also be allowed.

IV. Conclusion

For all the above reasons, it is respectfully urged that claims 1-53 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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